Multi-Scale Simulation of Hybrid Silicon Nano-Electromechanical (NEM) Information Systems

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Abstract:

This paper presents emerging NEM hybrid systems for advanced information processing and describes our recent attempts of developing new multi-physics simulation technologies for these NEM systems at micro-, nano- and atom-scales.

Keywords: *multi-scale simulation, NEMS, suspended-gate, non-volatile memory, phonon.*

1. Introduction

Silicon VLSI technology, developed and matured over the past decades, has been fully exploited to build the vast technology area of micro-electromechanical systems (MEMS). The MEMS market is projected to grow with the rate of 30 – 40 % per annum and reach ten billion dollars in 2015. In parallel with such a rapid expansion of the MEMS market, there have also been continuous efforts at making the MEMS smaller in order to boost the operating frequency to GHz and beyond. Figure 1 shows a recent miniaturization trend of semiconductor-based MEMS, superposed on the CMOS downscaling trend ('*More Moore*').

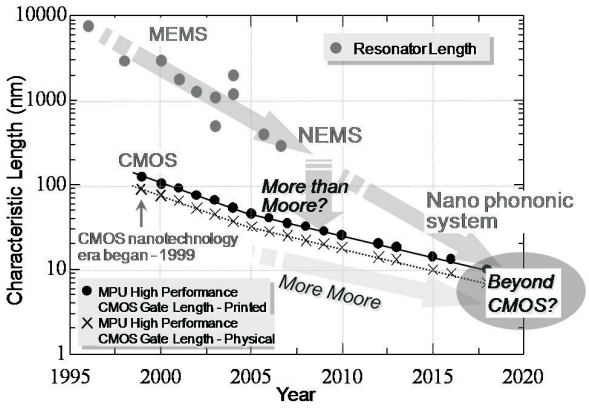
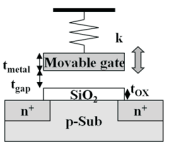
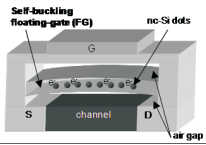
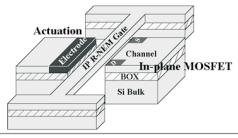


Fig. 1. Miniaturization trend of semiconductor-based resonators shown superposed on the CMOS downscaling trend from International Technology Roadmap for Semiconductors 2008.

Apparently, the MEMS technology has already entered a sub-μm regime and proceeds rapidly towards a nanometer-scale regime. The appearance of high-speed nano-electromechanical systems (NEMS) tempts to consider the hybridization of the NEMS and conventional silicon electronic devices because we expect such hybrid systems enhance scaling of functional density & performance while simultaneously reducing the power dissipation beyond the conventional CMOS-based systems. A variety of new hybrid NEM-MOS devices have recently been studied for logic, memory and sensing applications (see Table 1). A typical NEM hybrid device is a suspended-gate field-effect transistor (SG-FET) which features a movable gate suspended over the MOS channel with an air gap. The SG-FETs have already attracted an increasing interest due to the extremely abrupt switching with the subthreshold slope much smaller than the theoretical limitation of 60 mV/dec for MOSFETs.

Table 1. A variety of NEM – MOS hybrid devices.

Switch	Suspended-gate(SG)FET 	• Abrupt switching with S < 60 mV/dec • Very low leakage • Power management
Memory	• Self-buckling FG Memory • SG Si Nanodot Memory 	• Seriously nonvolatile • Fast write/erase operation • Conventional silicon process compatible
Sensor	• Resonant SG MOSFET • Vibrating body FET 	• Extremely high mass sensitivity of sub-attogram order • Co-integration with SOI-MOSFET circuits

For the memory applications, two types of novel high-speed and non-volatile NEM memory devices are currently researched to go beyond conventional Flash memory. As regards the sensing applications, an in-plane resonant suspended gate (RSG) MOSFET and a vibrating-body FET have been proposed very recently to achieve extremely high mass sensitivity. Along with such a rapid progress of the hybrid NEM devices, various attempts have been made to develop a new simulation technology suitable for the hybrid NEM devices. For the conventional MEMS, we have a number of powerful 2D/3D simulation tools based on the finite element method (FEM) analysis. In order to design and analyse our hybrid NEM-MOS systems, however, we need a new simulation technology, which solves the nonlinear mechanical equation electrostatically coupled to the carrier transport equations simultaneously. Furthermore, we have to build a multi-scale simulation, which facilitates to simulate the NEM hybrid systems at three different scales, i.e., microscale, nanoscale and atomscale (see Fig. 2). In the following sec-

tions, we focus on hybrid NEM-MOS memories and nano-phononic systems and present our recent attempts of developing the micro-, nano- and atom-scale simulation technology.

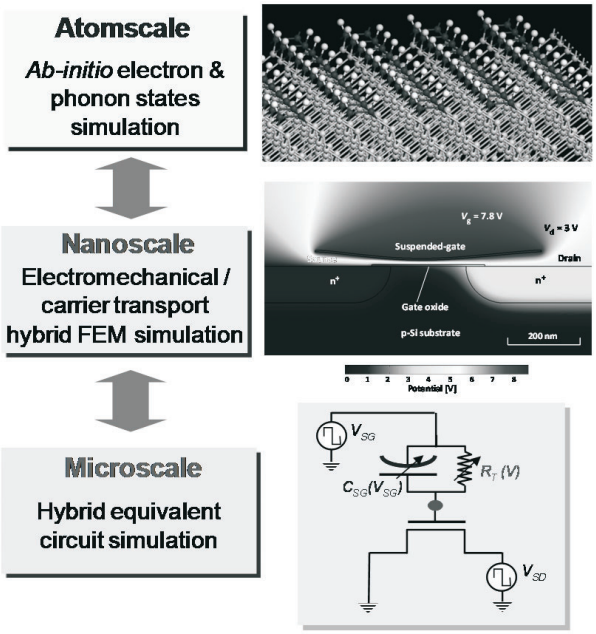


Fig. 2. Multi-scale simulation technology for hybrid NEM information devices and circuits.

2. Micro- and Nano-scale hybrid simulation of Si NEM-MOS systems

As the first attempt of the NEM-MOS hybrid devices, we have researched on a self-buckling floating gate (FG) NEM memory [1],[2]. This memory device features a buckled SiO_2 FG with a layer of embedded Si nanodots as charge storage (see Memory in Table 1). The buckled FG may be flip-flopped via the gate electric field, and its structural states are sensed *via* a change in the drain current of the MOSFET underneath. In order to design and analyse this NEM memory, we developed *nanoscale hybrid FEM simulation* that solves two- (or three-) dimensional Navier's equation for structural mechanics analysis of the self-buckling FG and Poisson's equation and the drift-diffusion equation for MOSFET electrical analysis simultaneously. The numerical simulation was conducted by using a general-purpose FED package COMSOL Multiphysics. Because three nonlinear equations need to be solved self-consistently in multiple degrees of freedom, it is inevitable that the numerical computation is time-consuming. Therefore 2D simulation is preferably used unless 3D natures are remarkable with the designed structure. Figure 3 shows the 2D carrier distribution calculated for the NEM memory at the OFF (a) and ON (b) states as well as the out-of-plane FG displacement (c) and the MOSFET readout current (d) hysteresis as a function of gate voltage. The threshold voltage shift and the ON/OFF current ratio were found approximately 1.6 V and 10^5 at V_g = 0 V. These results clarify that the bistable states of the NEM memory can be indeed read *via* the drain current. The associated switching voltage is around 10 V, which should be reduced further.

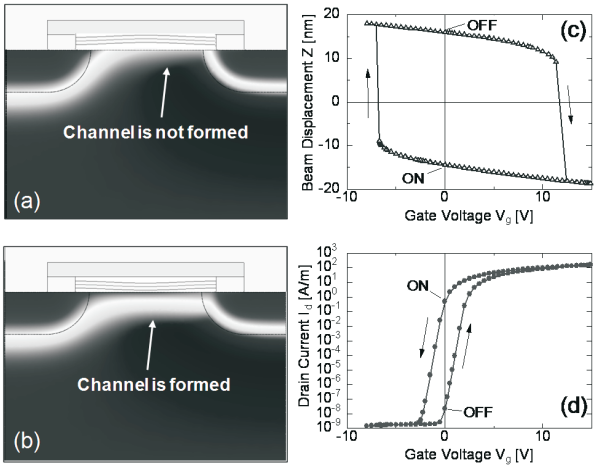


Fig. 3. 2D hybrid FEM simulation results for the self-buckling NEM memory with the FG of 1 μm in length and stored charge density of 8.5x10^{-8} C/m^2.

As an alternative NEM memory architecture, we recently proposed a suspended gate Si nanodot memory (SGSNM) [3], [4]. The SGSNM consists of a MOSFET as readout, silicon nanodots as a FG, and a clamped suspended gate (SG), which is isolated from the FG by an air gap and a thin tunnel oxide (Fig. 4(a)). For the programming (P) process, a negative gate voltage is applied, and the SG is pulled-in on the FG layer, resulting in electron injection from the SG into the FG. For the erasing (E) process, a positive voltage is applied, and the stored electrons are extracted from the FG. The SGSNM architecture enables to avoid an unfavourable trade-off between the ON/OFF current ratio and the P/E voltages and therefore facilitates low-power operation compared to the first NEM memory.

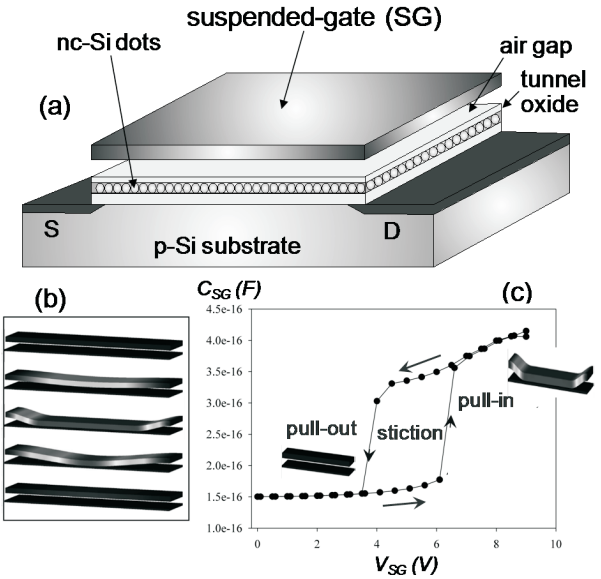


Fig. 4. A schematic suspended-gate silicon nanodot memory (SGSNM) (a) and the hysteresis in the suspended-gate to substrate capacitance (c) associated with the pull-in/pull-out operations (b).

In order to analyze the SGSNM cell, we developed the *Microscale hybrid equivalent circuit simulation* (the bottom of Fig. 1), which enables a large-scale cell array simulation in the future. It is, however, vital to build

a compact model of the SG including the tunnel injection and release processes. Therefore we first conducted a 3D FEM simulation to obtain full pull-in / pull-out characteristics for the SG (Fig. 4(b), (c)). The SG structural parameters were optimized in order to make the programming voltage as low as 6 V. The SG voltage dependences of the SG displacement and associated capacitance CSG were then calculated (Fig. 4(c)). It should be noted that the C_{SG}-V_{SG} curves show a remarkable hysteresis due to the SG stiction (static friction) onto the oxide. The calculated C_{SG}-V_{SG} hysteresis curve was modelled by using simple analytical formula. The same processes were conducted for negative gate voltages as well. Secondly, a compact model for the variable tunnel resistance was constructed based on the numerical simulation of quantum-mechanical tunnel current through the top gate oxide. The tunnel current density-voltage characteristics were calculated for a SiO_2 tunnel barrier by solving the 1D Schrödinger equation. The developed compact models were introduced into SmartSpice by using Verilog-A. By using the developed hybrid modelling, the P/E/R processes were successfully analyzed as shown in Fig. 5. The SG voltage and drain voltage waveforms are shown in Figs. 5(a) and (b), and the transient memory node voltage and MOSFET readout current are shown in Fig. 5(c) and (d), respectively. By assuming a 7-nm-thick tunnel oxide, the results show that the SGSNM achieves the P/E times of as short as 1.7 nsec, suitable for fast & non-volatile RAM applications.

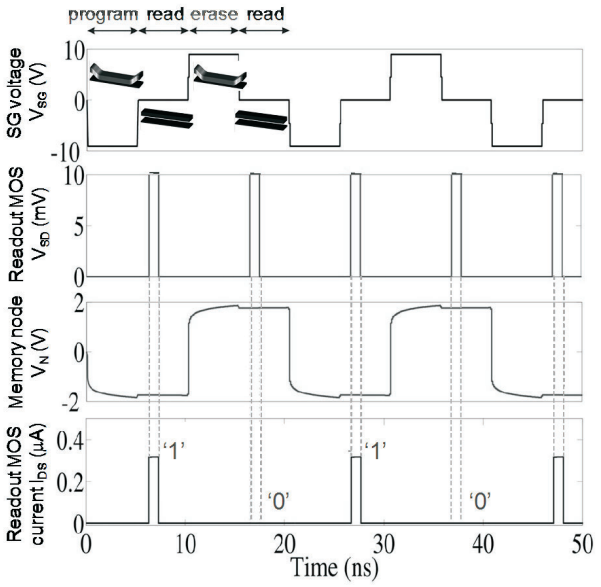


Fig. 5. Program/Erase/Read signal waveforms simulated for the SGSNM cell.

3. Towards atom-scale NEM systems

By downscaling the hybrid NEM systems towards a nanometer regime, we may explore a variety of novel functional devices such as NEM-SET (single-electron transistor). A suspended-gate SET (SGSET) is an apparent extension of the SGFETs which is expected to achieve a dramatic modulation of the Coulomb oscillation period as well as extremely fast switching. We have recently developed a hybrid NEM-SET equivalent circuit simulation successfully [5] by implanting the SET analytical model and the NEM compact model into SmartSpice in a similar manner described in Section 2.

However, we will need the atom-scale simulation framework for extremely scaled NEM systems whose electromechanical properties are described *via* low-dimensional phonons (nanophonons). Various new electron transport phenomena associated with nanophonons have been reported very recently, such as phonon blockade of single-electron tunnelling and quasi-ballistic transport due to suppressed optical phonons [6], which may be exploited to develop novel functional information devices.

As the first step towards the atom-scale NEM hybrid simulation, we developed the *ab initio* simulation of 'nanophonons' for the H-terminated freestanding ultrathin Si films of 3 to 10 atomic layers in thickness. The Si(0 0 1) 2x1 dimer structures were formed on the film surface, and the entire atomic structures were optimized by using the DFT (density-functional theory) simulator SIESTA. The atomistic properties of nanophonons were then calculated by using VIBRATOR, which is associated with SIESTA and based on the *ab initio* force-constant method.

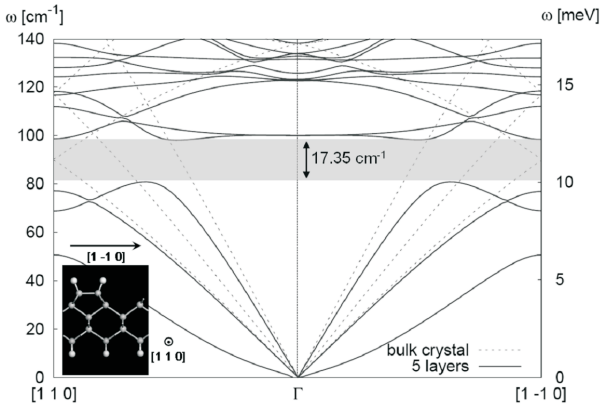


Fig. 6. Ab-initio simulation of nanophononic spectra for a hydrogen-terminated ultrathin Si film of 5 atomic layers in thickness. A phonon bandgap of 17.35 cm^{-1} is formed both in the (110) and (1-10) directions.

We observed for the first time that remarkable phonon bandgaps are formed for the films thinner than 7 atomic layers (see Fig. 6) [7]. The formation of the phonon bandgaps is caused by the Si dimers formed on the film surfaces in the (1-1 0) or (1 1 0) direction. Such nanophononic properties are quite different from those for bulk silicon and may be further investigated as one of approaches to nanoscale thermal management and novel energy transfer interactions in the '*Beyond CMOS*' information devices.

4. Conclusion

Various attempts have been made to develop new micro- and nano-scale multi-physics simulation technologies suitable for the emerging NEM-MOS hybrid devices. The micro-scale hybrid circuit simulation with compact NEM models developed by using 3D FEM simulation provides a fast and practical approach and has been applied to the NEM memory devices successfully. The preliminary atom-scale simulation revealed the formation of phononic bandgaps in atomically thin Si films.

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