

LINEARIZED SETTling ERROR CALIBRATION FOR A PIPELINE A/D CONVERTER USING NON-SLEWING AMPLIFIERS

Sung-Wook Jun, Keita Yasutomi, Shinya Itoh, Shoji Kawahito

Abstract:

In this paper a new method of linearized settling error calibration for a pipeline A/D converter is proposed. The pipeline A/D converter employs non-slewing amplifiers for linearizing the settling error. A prototype 15b pipeline A/D converter was fabricated in 0.25 μm process. The calibration is carried out by adjusting gradients and offsets of the linearized settling error. The calibration of the settling error improves the SNDR and SFDR from 68 dB and 74 dB to 72 dB and 88 dB, respectively, at 35MS/s.

Keywords: CMOS integrated circuit, pipeline A/D converter, non-slewing amplifier, settling error, calibration

1. Introduction

Analog-to-digital converters (ADCs) are one of the important building blocks in modern electronics systems, which can transfer from analog information to digital signals profoundly affects system architectures. Among them, pipeline ADCs are widely used for various applications, which require analog-to-digital converters with high speed(>10MSPS), medium resolution (8-14b) and reasonable low power dissipation. With the need of increased speed and integration density in the state-of-the-art digital IC systems, recent digital CMOS technology is continuously down-scaling into submicron region. Even though digital systems are well following this trend of technology in terms of area and power, analog designs are faced with the design challenge of voltage headroom which invokes deterioration of power efficiency and speed.

In order to relax inherent problems of analog design, digitally assisted architectures which seem to have been focusing on various nonlinear calibration schemes are recently reported [1]-[4]. In this work, we propose linearized settling error calibration with non-slewing amplifiers.

2. Linearized Settling Error Correction

The general errors of the pipeline A/D converter can be categorized into linear error and non-linear error. Capacitor mismatch and finite gain error of amplifiers can be regarded as linear errors in pipeline A/D converter. On the other hand, one of the non-linear errors is incomplete settling error which makes power efficiency worse and difficult to apply calibration. In order to make this settling error feasible to apply calibration, we need to linearize this non-linear error. In this section, a design technique to alleviate non-linearity of settling error and mathematical formulation of the proposed calibration is described.

2.1. Non-slewing Amplifier

The non-linearity of the settling error is mainly caused by the slewing of amplifiers. A capacitance-coupling push-pull amplifier shown in Fig. 1 can suppress the slewing in transient response, and provide large output current with little static power dissipation. The gates of MP1 and MN1 are capacitively coupled to the input, which work as level shifters for the input signal to drive MP1 and MN1 complementarily.

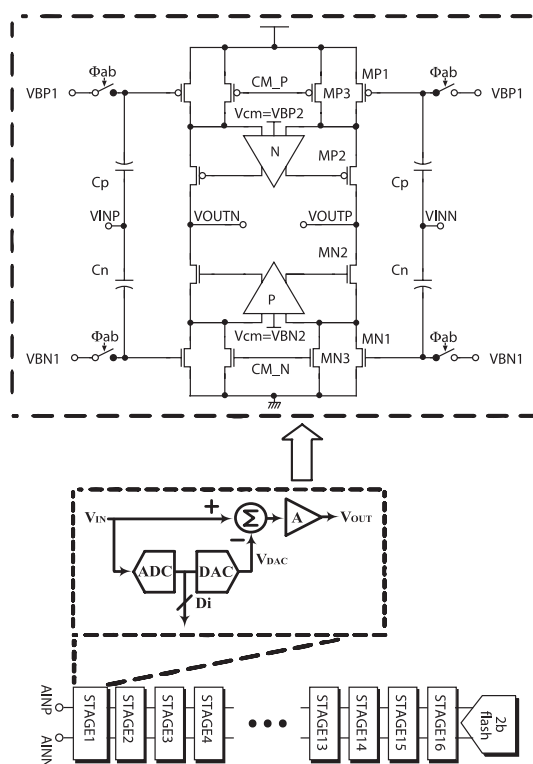


Fig. 1. Non-slewing amplifier.

2.2. Errors in Digital Domain

Fig. 2 shows the voltage transfer curve and settling errors. The i-th stage residue voltage is expressed as

$$V_{OUT}[i] = (1 - E_{st}[i]) \left\{ V_{IN}[i] \frac{(2 + a_i)}{\left(1 + \frac{1}{A_V}\right) + \frac{a_i + 1}{A_V}} - D_i V_{REF}[i] \frac{(1 + a_i)}{\left(1 + \frac{1}{A_V}\right) + \frac{a_i + 1}{A_V}} \right\} \quad (1)$$

where, $E_{st}[i]$ is the settling error[%], A_V is finite gain error and a_i is capacitor mismatch factor of the i -th stage. All values are represented by digital domain. Equivalently, (1) can be approximated to

$$V_{OUT}[i] = V_{IN}[i](1 + g_i)(2 + a_i) - D_i V_{REF}[i](1 + g_i)(1 + a_i) \quad (2)$$

where, $(1+g_i)=(1-E_{st}[i])/(1+(a_i+2)/A_V)$. Using (2), the error in digital domain is expressed as

$$E_i = D_i V_{REF} [i] \omega_i - V_{IN} [i] \gamma_i \quad (3)$$

where, $\omega_i=g_i+a_i(1+g_i)$ and $\gamma_i=2g_i+a_i(1+g_i)$. By subtracting summed all stage error values from digital output code, error corrected final digital output can be obtained.

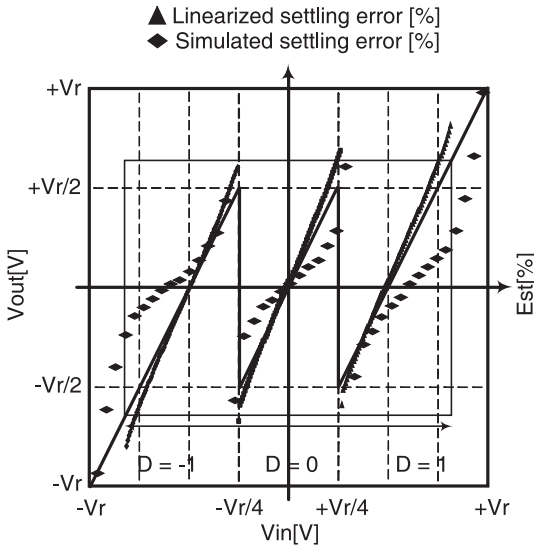


Fig. 2. Voltage transfer curve and settling error.

2.3. Error Correction Algorithm

Fig. 3 depicts a block diagram of data processing. Error correction logic has been implemented off chip on a PC. Fig. 4 shows the two types of pre-estimated settling error applying to error correction algorithm. Each definition of settling error is divided into three regions depending on the input value of each stage. According to Fig. 4 (a) which assumes same shape in each three regions, each three region have same gradient. The settling error in this case can be expressed,

$$E_{ST} [i] = \begin{cases} G \times V_{IN} [i] & (D = -1) \\ G \times V_{IN} [i] & (D = 0) \\ G \times V_{IN} [i] & (D = 1) \end{cases} \quad (4)$$

where, G is a gradient of each region.

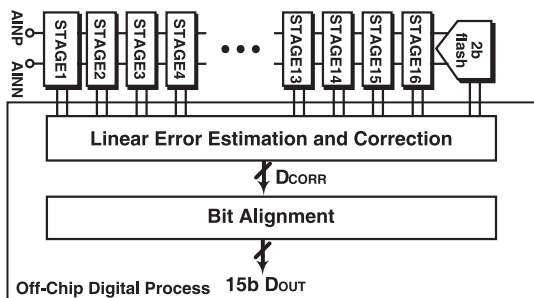


Fig. 3. Block diagram of ADC.

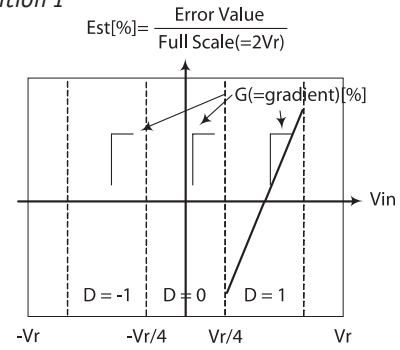
Unexpectedable component mismatch and offset can cause variation of gradient and offset. Consequently, pre-estimated settling error can have three differential

gradients and offsets in each region which is shown in Fig. 4 (b). The settling error can be expressed,

$$E_{ST} [i] = \begin{cases} G_1 \times V_{IN} [i] - Offset_1 & (D = -1) \\ G_2 \times V_{IN} [i] - Offset_2 & (D = 0) \\ G_3 \times V_{IN} [i] - Offset_3 & (D = 1) \end{cases} \quad (5)$$

where, G_1, G_2 and G_3 are the gradients of each region and $Offset_1, Offset_2$ and $Offset_3$ are the offsets of each region, respectively.

(a) Definition 1



(b) Definition 2

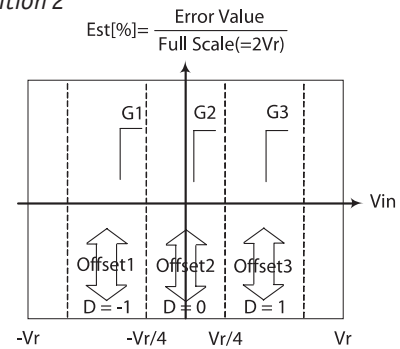


Fig. 4. Settling error definition.

3. CMOS Prototype Design

The pipeline A/D converter uses a SHA-less 1.5b front-end stage with non-slewing amplifier, followed by 1.5b stages from 2 to 16, and 2b flash stage at the end. The prototype A/D converter was fabricated in a 2.5 V, 0.25 μ m, 5M1P CMOS technology. Capacitors are implemented using metal-insulator-metal (MIM) structures. It occupies an active area of 1.6 mm²×4.0 mm². All measurements are performed on the chip-on-board (COB). The chip microphotograph is shown in Fig. 5.

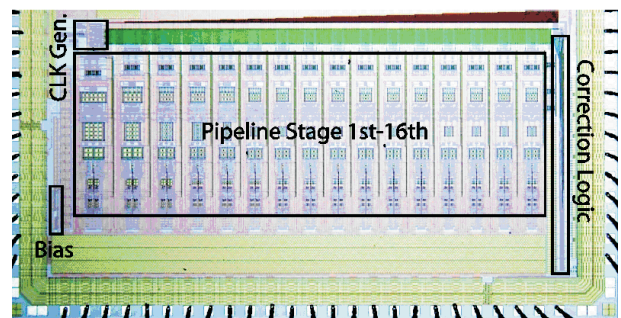


Fig. 5. Chip microphotograph.

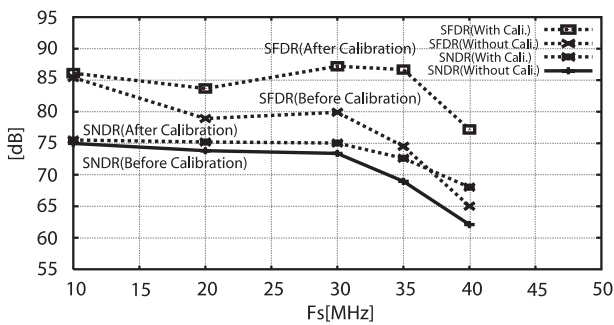


Fig. 6. Before & after calibration with Definition 1.

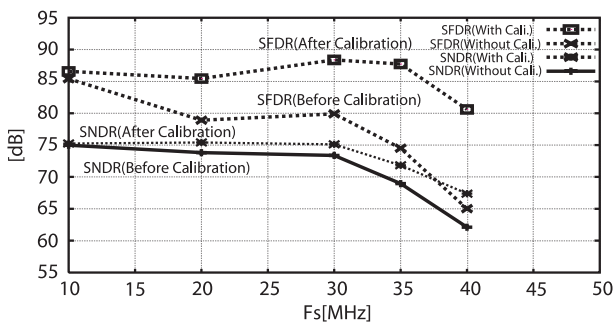


Fig. 7. Before & after calibration with Definition 2.

Table 1. Summary.

	Before Cali.	After Cali.
Process	P0.25 μm CMOS 5M1P	
Supply	2.5 V	
Resolution	15 bits	
Input Range	3.2 Vpp	
Sampling Rate	35 MHz	
Chip Area	1.6 mm ² ×4.0 mm ²	
Power	123 mW	
FOM	0.87 pJ/conversion-step	
DNL	-0.42LSB / +0.25LSB	
INL	-2.5LSB / +2.5LSB	
SNDR	68.9	71.9
SFDR	74.5	88.0

4. Measurement Results

First of all, the coefficient G of Equ. (4) is applied to digital calibration. Fig. 5 shows signal-to-noise-and-distortion ratio (SNDR) and spurious free dynamic range (SFDR) before and after calibration as a function of conversion rate at an input signal frequency of 10 MHz. The SFDR improves from 74 dB to 86 dB before and after calibration, respectively, and SNDR improves from 68dB to 72 dB before and after calibration, respectively, in 35MSample/s. From Equ. (5), the differential gradients and offsets are applied to digital calibration. Fig. 6 shows SNDR and SFDR before and after calibration as a function of conversion rate where input signal frequency is 10 MHz. The SFDR improves from 74 dB to 88 dB before and after calibration, respectively, and SNDR improves from 68 dB to 72 dB before and after calibration, respectively, in 35Msample/s. Table 1 summarizes the measured performance of the prototype.

5. Conclusion

A prototype 15b pipeline A/D converter with non-slewing amplifier is tested for settling error correction. The

calibration of linearized settling error is accomplished by the gradients and the offsets of settling error. Experimental results show that the calibration improves the SNDR and SFDR of the prototype A/D converter 4 dB and 14 dB, respectively, at a sample rate of 35MS/s. But it shows severe degradation in both of SNDR and SFDR over 35 MHz of sampling frequency. It invokes that even though the performance is enhanced by calibration, the high sampling frequency raise the noise floor. Due to increased noise floor, It is not enough to prevent performance keeps going down by calibration of linearized settling error over 40MS/s.

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